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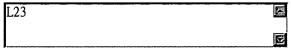US Patents Full-Text Database
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L18	l16 and count$3	183	L18
L17	(multi near1 thread$4 or thread$3) near5 (plur$7 or multiple or two) and l4	23	L17
L16	(multi near1 thread$4 or thread$3) near5 (plur$7 or multiple or two) and l3	287	L16
L15	L1 and l4	6	L15
L14	L1 and l6	0	L14
L13	L8 and l6	0	L13
L12	L8 and l5	2	L12
L11	L8 and l4	0	L11
L10	L8 and l3	17	L10
L9	L8 and l2	44	L9
L8	L7 and count$5 near6 (cycle$1 or clock$3 or tim$5)	201	L8
L7	(lead$3 or trail$4 or first or primary or second) and l1	2762	L7

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L4	(719/331)![CCLS]	263	L4
L3	(718/107,108)![CCLS]	771	L3
L2	(712/3-300)![CCLS]	10293	L2

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L1	(multi near1 thread$4 or thread$3) near5 (plur$7 or multiple or two) and (replicat$4 or duplicat$4 or cop$3 or identical) near4 thread$3	3047	L1

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1 **Transient fault detection via simultaneous multithreading**
Reinhardt, S.K.; Mukherjee, S.S.;
Computer Architecture, 2000. Proceedings of the 27th International Symposiu
on , 10-14 June 2000
Pages:25 - 36

[Abstract]   [PDF Full-Text (1412 KB)]   **IEEE CNF**

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2 **A nested invocation suppression mechanism for active replication fa tolerant CORBA**
Deron Liang; Chen-Liang Fang; Chyouhwa Chen; Fengyi Lin;
Software Engineering Conference, 2002. Ninth Asia-Pacific , 4-6 Dec. 2002
Pages:117 - 125

[Abstract]   [PDF Full-Text (409 KB)]   **IEEE CNF**

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3 **A nested invocation suppression framework for active replication fa tolerant CORBA**
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Pages:757 - 762

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4 **A study of slipstream processors**
Purser, Z.; Sundaramoorthy, K.; Rotenberg, E.;
Microarchitecture, 2000. MICRO-33. Proceedings. 33rd Annual IEEE/ACM
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